# The Ontario TECHNOLOGIST

VOLUME XXXVI NUMBER 1 JANUARY/FEBRUARY 1994

*Electronics*

## Voltage contrast techniques for integrated circuit troubleshooting

*Page 6*

# Integrated circuit troubleshooting using voltage contrast techniques

By Charles O'Dale, CET

Mr. O'Dale's paper appeared in System Reliability, published for a conference last year by Bell Northern Research. It is reproduced with BNR's kind permission.

***Abstract:*** *Voltage Contrast Testers are assigned at Bell Northern Research and Northern Telecom Ottawa for interior diagnostic probing of custom integrated circuits. This paper will summarize the techniques used and developed in our laboratories using this contactless probing system.*

## Introduction

Once a failure in a VLSI (Very Large Scale Integrated Circuit) device has been revealed by external electrical testing, isolating the fault within the integrated circuit (IC) requires probing of its internal circuitry. Scanning electron microscopes (SEM) specializing in voltage contrast (VC) are used at BNR and NT for contactless, damage free probing within the IC. These microscopes have the ability to detect variance of voltages on the internal conductors of the IC and display the information as voltage contrast images and waveforms for documentation and classification of IC failures. The techniques developed are described, followed by a case study using these techniques [1].

## Voltage Contrast

When the electron beam of the SEM scans a section of the IC, secondary electrons (SE) are emitted. The brightness of the image increases with the number of emitted SE. The voltages on an integrated circuit set up surface electrostatic fields which influence the paths of the SE. Regions with a positive voltage attract a proportion of the SE back to the surface of the IC. As the voltage increases, more and more SE are attracted in this way. These fields modulate the number of SE arriving at the SEM detector. Consequently, the more positive the voltage, the darker the image is of the associated region. This raw voltage contrast is nonlinear. To make quantitative voltage measurements, this characteristic is linearized by placing a filter electrode between the IC and the SEM detector. The voltage applied to this filter sets up a secondary electron retarding field, forcing the SE to climb a small potential barrier. A feedback loop varies the voltage on the filter to maintain a constant number of detected SE. The voltage variation on the filter electrode will track the voltage variation on the monitored IC surface [2].

## Image Mode

Applying power to the IC and observing the IC in image mode reveals the DC conditions on the surface layers of the chip. They are displayed by bright (more negative) and dark (more positive) contrast superimposed on the image of the surface metal tracks. This is an immediate indication to the troubleshooter of the DC voltage conditions on the monitored cells [3].

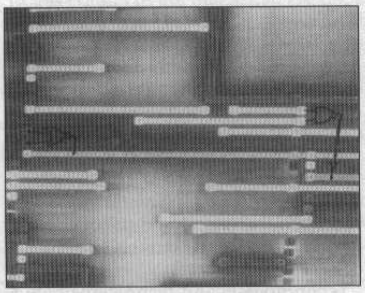


*Image Mode*
*Figure 1 illustrates the voltage contrast caused by the influence of the DC voltages on the various metal conductors of the IC, the dark colour being more positive than the bright coloured areas (5V in this case). Note the center horizontal grey coloured conductor. This implies that it is stuck at mid rail (ie: 2.5V).*

Running the test facility at speed, the contrast of the signal paths will turn a shade of grey (between the dark and bright colours of positive and negative) dependent on the duty cycle of the signal. In addition, a pattern caused by the test frequency beating with the SEM scan rate frequencies will also be superimposed on the signal track. This is a form of voltage coding. The DC conditions that exist and which tracks conduct signals are revealed. The different patterns developing on the signal tracks are caused by the frequency beating with the scan rates of the SEM. The different patterns imply different frequencies. This technique is used for signal tracing and determining the circuit areas which are active.

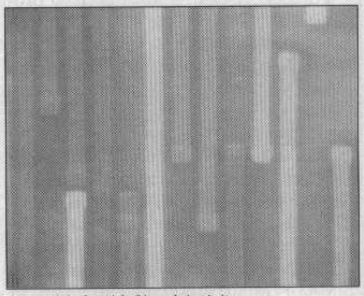
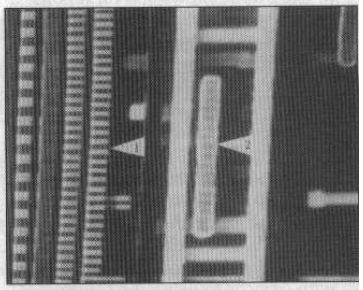


*Image Mode with Signal Activity*
*Figure 2 documents the DC voltages on the IC conductors indicated by the shades of contrast. The grey colours superimposed with a grid pattern on some tracks reveal AC signal activity. This information gives the designer an immediate indication of cell functionality.*

## Slow Scan Image Mode

By single-stepping the test facility exercising the IC under test, the circuits that carry signals will switch logic states at the rate determined by the test facility. The changing logic states can be documented by observing the changing contrast on the signal paths. In addition, when we slow the scan rate of the image monitor and single step the circuit a number of times per verticle scan, a logic state map of the circuit is revealed on the switching conductors of the circuit (see Figure 3). This technique will document the switching rate of the circuits under observation as well as circuit operation status.

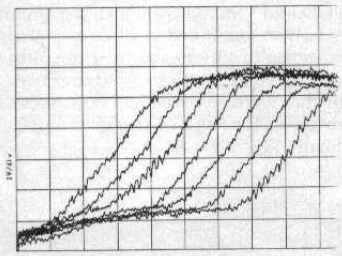


*Slow scan image*
*Figure 3 documents different clock rates across the area scanned illustrated by the changing voltage contrast. This information can be used by the troubleshooter to determine if the circuits under test are operating at the correct frequencies. This micrograph indicates two clock rates (area 1 indicated).*

*and a circuit not switching to its full rail to rail voltage (area 2).*

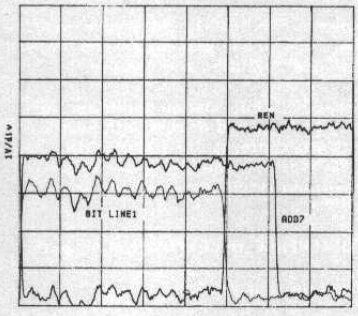
### Waveform Mode

The troubleshooter can use the voltage contrast SEM in the same way as a single probe sampling oscilloscope when probing the micron size conductors of the IC in waveform mode. The electron beam pulse is triggered by the test pattern used by the IC under test. The signal voltage probed at the specific area of the IC is accurately derived by monitoring the feedback control of the electron energy filter, and by further digital processing. The electron energy filter feedback output is a voltage proportional to the test point voltage at the instant of sampling and is used to generate the waveform display. The SEM can resolve waveform edges to <100ps, time to <100ps and voltage to <20 mV [4]. The displayed waveforms can be stored for later comparison of edge timing, signal swing, etc.



500 ps/div

*Waveform mode*
*Figure 4 is a family of waveforms that document the propagation delay between inverter circuits of a ring oscillator. For clarity, only the rising edges of alternate cells are illustrated. The propagation delay between each cell containing two CMOS transistors is averaging 220/2 • 110 ps and the rise times are averaging 800 ps.*



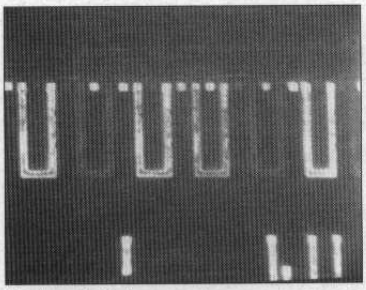

200 ns/div

*Waveform Mode*
*Figure 5 documents a memory circuit with an address signal changing state AFTER the read enable signal is activated. This information enabled the designer to modify his design to correct this malfunction.*

### Stroboscopic Mode

To produce a strobo-voltage map, the electron beam is pulsed in the same way as for waveform mode, but the pulse phase is held constant while the image is recorded. The electron beam is scanned as for a real time image and the result is a voltage map which shows the circuit at a specific window of time (ie 200 ps) relative to the trigger (ie 5 us delay) superimposed on the surface of the integrated circuit.

These images will reveal relative logic states and transition times of the circuit under test. A direct comparison of switching edges to a specific time or monitored waveform can be documented for analysis. Events happening on other parts of the circuit at other times are revealed by changing the relative delay of the sample window. In this way the designer can document events to 200pS on the circuit under observation.

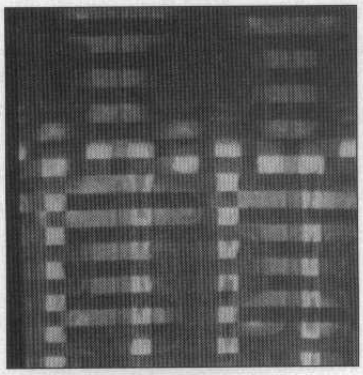


*Stroboscopic Mode*
*Figure 6 is a stroboscopic image of an inverter in the process of logic state transition. Note the bright and dark colours indicating the circuit resting at the rail voltage. The grey coloured conductor indicates a circuit part way through its switching process. The time window is 200 pS wide. Changing this window +/- in time will show this transition edge propagating through the circuit.*
*Note that Figure 4 is a waveform depiction of this circuit performance.*

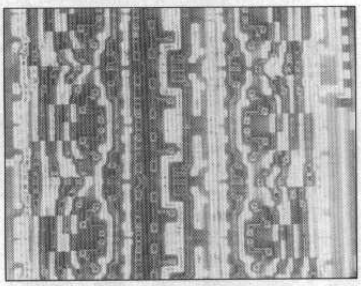
### Voltage Coding Mode

When the scan rate of the SEM is synchronous with the signal on the device under test, a stationary grid pattern will appear superimposed on the conductor carrying the signal. This is accomplished by triggering a burst oscillator with the line scan rate of the SEM and image monitor, the burst output being the signal exercising the device. The pattern on the image will reveal the signal conductor tracks, the inversions of the signal, multiples of the frequency rate, etc. The troubleshooter has an immediate indication of the signal status on the monitored circuitry.

By experiment, the maximum frequency resolution of the voltage coding mode at normal SEM scan rates is 6.14 MHz (determined by one transition per image pixel) [5]. The minimum resolution at normal scan rates is 8 KHz (determined by the physical size of the image monitor). By changing the scan rate of the monitor, the minimum resolution can be improved to less than 1 Hz.



*Voltage Coding*
*Figure 7 documents how Voltage Coding Mode can be used by the troubleshooter to resolve logic states. As time passes left to right, a signal inversion is documented between the two circuits operating at 1 MHz. The inversion is displayed by the changing voltage contrast on each horizontal coding line. Also, this inversion can be resolved in lower layer metals under passivation. Note that DC voltages cannot be resolved on these buried conductors.*



*Reduced Scan Rate Voltage Coding*
*Figure 8 illustrates how Voltage Coding will document the different clock rates existing across the scanned area. This information can be used by the troubleshooter to determine if the circuit under test is operating at the correct frequencies. This micrograph also documents the existing DC voltage conditions.*

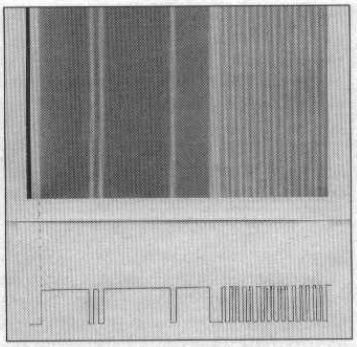
### Pseudo Logic Analyzer Voltage Coding Mode

Expanding on the voltage coding option, if a whole software loop can finish within one line scan of the SEM, a voltage contrast image of the logic states vs time can be displayed [6-7]. To synchronize the scan rate of the SEM with the software loop a pulse generator is triggered by the horizontal 62.6 uS scan pulse. This pulse triggers the beginning of the software loop in the supplied tester that drives the IC under test. The image of the software loop on the SEM monitor is centered by adjusting the duty cycle of the single burst from the burst generator. With this technique, a transformation of time

dependent signals to spatial dependent signals is carried out that allows the observation of logic states on the IC v.s. time. This enables a logic analysis of the software loop in various IC cell nodes by observing the voltage contrast representation of voltage levels vs time on the metal conductors synchronous with the line scan of the SEM. A translation of the voltage contrast pattern into a logic plot reveals the signal content of any monitored conductor at any time within the software loop. Forcing the IC under test to switch between failure and nonfailure modes will produce voltage changes on the failing cell outputs that are out of sync with the nonfailure mode. The malfunctioning circuit producing the transient nonsynchronous outputs will reveal itself as a flashing Voltage Contrast image on the failing signal conductor when observing this IC cell in real time image mode. This observation will document the failing cell's location and the approximate time of the failure within the software loop.

For the software loop to be resolved on the image monitor, the following conditions must apply [7]:

1. each SEM horizontal scan trigger must reset the software loop in the IC tester,
2. the loop must cycle once and hold,



*Logic Analyzer Voltage Coding*
*Figure 9 is a voltage image contrast image of a logic analyzer pattern on a single IC conductor. The logic translation can be plotted with the dark areas as logic 1 and the bright as logic 0. The troubleshooter using this analysis method can determine if this is, in fact, the proper logic pattern that is output by the observed circuit.*

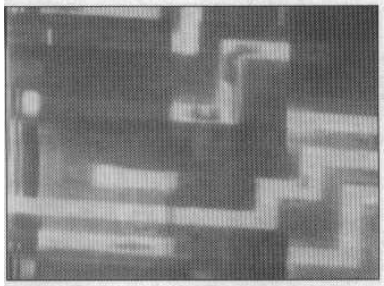
3. the loop must be shorter than the SEM horizontal scan rate, in this case 62.6 us, to complete its cycle within each scan line of the image monitor,
4. the clock driving the software loop must be less than 6 MHz for the logic transitions to be resolved on the image monitor.

## Case Study

The unit failed a PSCAN driven DC test on the Teradyne A500 tester as well as on two different bench testers. The unit functioned to specifications with an open circuit load but malfunctioned when loaded with 50 pF. The unit was set up in the Voltage Contrast Lab and exercised so that it could be observed in passing and failure modes [8]. The unit was first monitored using the pseudo logic analyser mode to confirm the existence of a failure in the suspected circuitry. A transient failure (glitch) was observed and this failure traced back to a malfunctioning circuit (Figure 10). The image of the glitch also identified the approximate time of the failure within the software loop. This circuit was then probed in waveform mode to determine the exact time of the failing clock edge (Figure 11 & 12).

Analysis of the failing clock edge revealed a transient superimposed on the signal, possibly from a power surge. The VDD and VSS rails of the failing circuit were then monitored in waveform mode for noise or glitches at the time of the identified failing clock edge. Power glitches were observed and documented at the exact time of the chip failure (Figure 13).

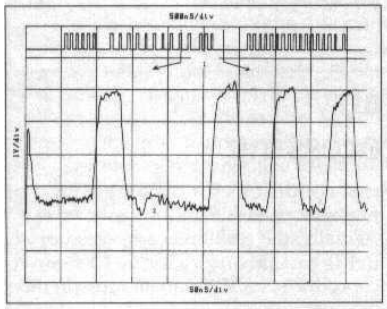
1-glitch



1-glitch

*Figure 10*
*Voltage Coding—Temporal Vs Spatial:*
*This micrograph documents a glitch (indicated as the grey area of the logic pattern) on specific conductors during a specific time within the software loop. The glitch, conspicuous by its grey colour, is caused by randomly high and low voltage averaged over a time span. The physical location of the malfunctioning circuit is identified as well as the approximate time of the fault within the software loop, represented by the X axis of the picture.*

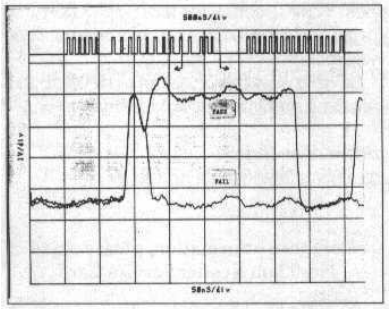
500 ns/div



50 ns/div

*Figure 11*
*Waveform Documentation—Clock: The time base for the logic state plot of the software loop (top) is 500 ns/division. This illustrates the whole loop. The time area of the glitch happening within the software loop is expanded to 50 ns/division (1). The pulse in the VSS level of the expanded clock waveform (2) indicates the time of the glitch in relation to the whole software loop.*

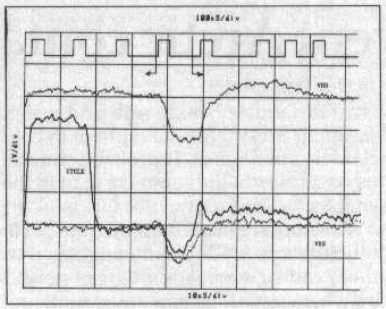
500 ns/div



·50 ns/div

*Figure 12*
*Malfunctioning Circuit Output—This waveform plot with the exact expansion factor of Figure 11, documents the passing and failing output of the cell with changing VDD, 4.2 and 3.9 Volts respectively.*

100 ns/div



10 ns/div

*Figure 13*
*VDD & VSS Glitch: This expanded plot of the glitch area of the software loop illustrates the power surges on the VDD and VSS rail within the failing logic circuitry of the unit at the exact time of the failure.*

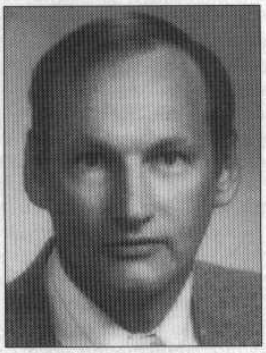
The malfunctioning circuit had changed to failure mode without any observed anomalies in its input signals. The cause of the failure is possibly a power/ground noise issue. The microsurgery lab added extra VDD supply connections to the failing area of the unit. The internal transients were marginally reduced requiring a larger adjustment on the external VDD supply to exhibit the same failure mode.

## Conclusion

The presented Voltage Contrast Scanning Electron Microscope probing techniques, used separately or in combination, provide a troubleshooting capacity for internal circuitry of VLSI. The VC SEM is essential for design fault and failure analysis troubleshooting of advanced semiconductor IC devices at Bell Northern Research and Northern Telecom.

### References


1. T.R. Touw, P.A. Herman and G.V. Lukianoff, "Practical Techniques for Application of Voltage Contrast to Diagnosis of Integrated Circuits, "SCANNING ELECTRON MICROSCOPY/1977 Vol. I p. 177-182.
2. A.R. Dinnis, "Detectors for Quantitative Electron Beam Voltage Measurements," SCANNING MICROSCOPY, Vol 2 p.1407-1418.
3. D.L. Crosthwait and F.W. Ivy, "Voltage Contrast Methods for Semiconductor Device Failure Analysis," SCANNING ELECTRON MICROSCOPY/1974 Part IV p. 935-940.
4. J. Watts, "Accuracy of Timing Measurements Using an E-Beam Tester," ISTFA/90 p.337-344.
5. H.P. Feuerbaum and K. Hernaut, "Application of Electron Beam Measuring Techniques for Verification of Computer Simulations for Large-Scale Integrated Circuits," SCANNING ELECTRON MICROSCOPY/1978 p.795-799.
6. G.V. Lukianoff and T.R. Touw, "Voltage Coding: Temporal Versus Spatial Frequencies," SCANNING ELECTRON MICROSCOPY/1975 p.405-471.
7. M. Ostrow, E. Menzel, E. Postulka, S. Gorlich, E. Kubalek, "IC-Internal Electron Beam Logic State Analysis," SCANNING ELECTRON MICROSCOPY/1982 p. 563-572.
8. E. Menzel, E. Kubalek, "Electron Beam Test Techniques for Integrated Circuits," SCANNING ELECTRON MICROSCOPY/1981 p.305-322.


*Charles O'Dale has been with Bell Northern Research since 1970, when he worked on analog carrier and digital switching systems. He now runs an integrated circuit diagnostics lab which specializes in SEM analysis of IC failures. Before his employment at BNR, he was an electronic warfare technician in the Royal Canadian Navy.*

*His hobbies include flying and sailboat racing; he owns an airplane and a sailboat. He presently serves with the Canadian Naval Reserve.*